Three Phase Cascaded H-Bridge Multilevel Inverter with Ac Source

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Abstract— this paper presents a multilevel inverter model working in H-bridge topology. The multilevel model comprises of several H-bridge models consisting of MOSFET/IGBT that are cascaded to get desired number of levels. The inverter is fed from existing AC supply which is rectified and fed to inverter. The inverter is controlled using PWM technique. This model is proposed for speed control of AC motors. Also the TOTAL HARMONIC DISTORTION (THD) waveform is studied. In order to study the proposed topology and proposed system several simulation results are presented.

Keywords — Multilevel inverter-bridge, PWM technique, THD, Speed control, cascaded, AC source, MOSFET, IGBT.

1. INTRODUCTION

Multilevel inverters have become a fascinating field of study for their industrial application. These converters allow the synthesizing of a sinusoidal voltage waveform starting from several levels of dc voltages. The important advantages of multilevel inverters are reduced switchinglosses, low rate of change in voltagesand reduced common mode voltages.There are three basic topologies of multilevel inverters. They are Diode clamped, flying capacitor and H-bridge topologies. The main industrial applications of multilevel inverters are speed control of AC motors and Induction heating. [1]

For HIGH-POWER applications, multilevel inverter structures have the particular advantages of operation at high dc-bus voltages, achieved using series connections of switching devices, anda reduction in output voltage harmonics, achievedby switching between multiple voltage levels. The two most common multilevel inverter topologies are the diode-clamped inverter and the cascaded inverter.

Theflying capacitor converter is another of the important multilevel topologies. This multilevel structure does not need clamping diodes, but still has Dc-link voltage unbalancing problems. The diode-clamped multilevel converter is one of the most used multilevel topologies. This power converter consists of two capacitor voltages in series and uses the central tap as the neutral. However, this power converter needs a complex control system in order to balance the capacitor Voltage. The diode-clamped inverter uses a single dc bus that issubdivided into a number of voltage levels by a series string ofCapacitors. A matrix of semiconductor switches and diodes allows each phase-leg output to be switched to any of these voltage levels. Pulse width-modulation (PWM) principles for this topology are fairly well established, but some modification of the basic modulation process is generally required to maintain balanced dc voltages across the series Capacitors using redundant switching states.

The third important multilevel topology is the cascade H-bridgeinverter. This last multilevel inverter hasbecome very important due to its modular structure andeasiness of operation. Another advantage is that does nothave the voltage balancing problems common to dccapacitors of diode-clamped or flying multilevel inverter.The cascaded inverter uses series strings of single-phase full bridge inverters to construct multilevel phase legs. A particular advantage of this topology is that the modulation, control, and protection requirements of each bridge are modular. However, each single-phase inverter requires its own isolated dc supply, typically derived from a multi winding low-frequency transformer or high-frequency dc-to-dc converters. This complexity has generally restricted cascaded Inverters to the higher power range where several switched output voltage levels are needed and a diode-clamped structure is unsuitable because of the difficulty of balancing the series dc capacitor voltages. [2]

2. H-bridge multilevel inverter

A separate dc source is connected to a single-phase full-bridge or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the switches. For a two level output to obtain $+V_{dc}$ two switches are turned on, whereas $-V_{dc}$ can be obtained by turning on another two switches. By turning on all the switches , the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

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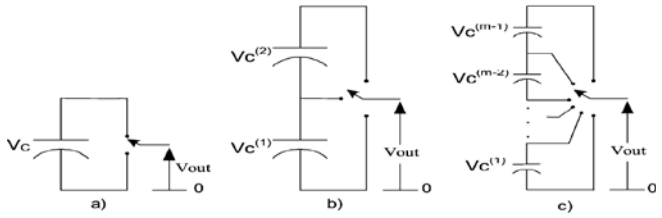

Fig 2.1 MULTILEVEL INVERTER CHARACTERISTICS

The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

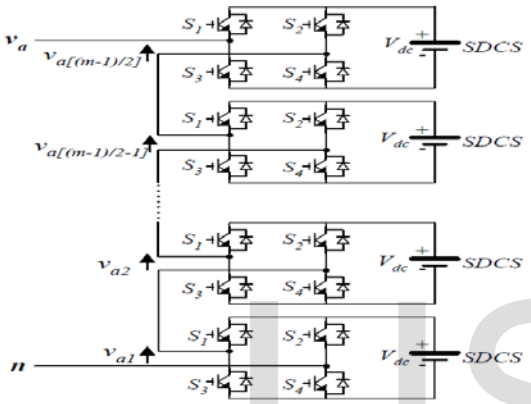

Fig2.2H-BRIDGE TOPOLOGY OF A MULTILEVEL INVERTER

The multilevel cascade inverter synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. A series of single-phase full bridges makes up a phase for the inverter. A single-phase multilevel cascade Inverter topology is essentially composed of single identical phase legs of the series-chain of H-bridge inverter, which can possibly generate different output voltage waveforms and offers the potential for ac system phase-balancing. This feature is impossible in other Voltage source control topologies utilizing a common dc link. Since this topology consists of series power conversion cells, the voltage and power level may be easily amplified. The dc link supply for each full bridge inverter is provided separately, and this is typically achieved using diode rectifiers without using the single-phase transformer. The converter topology is based on the series connection of single-phase inverters with separate dc sources the resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. For example in a five level cascaded inverter each single-phase full-bridge inverter generates five voltages at the output:+Vdc, + 2vdc, 0,-Vdc and -2Vdc.
As Multilevel inverter is made up of semiconductor switches which are very sensitive to disturbances and become less

tolerant to power quality problems such as under voltage and over voltage. So a suitable controller is required to maintain constant voltage.

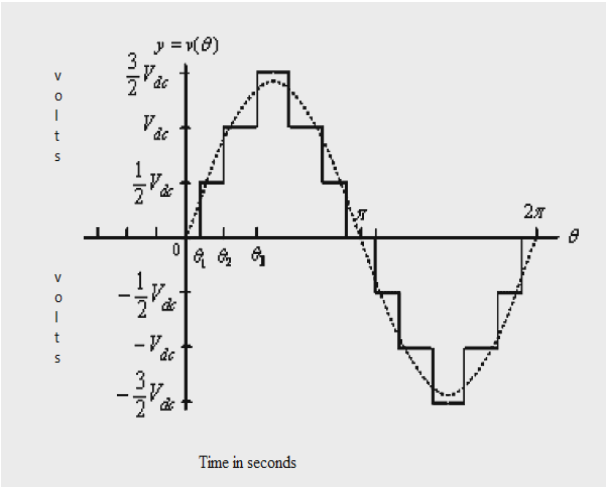

Fig 2.3 OUTPUT WAVEFORM OF A MULTILEVEL INVERTER

3. CASCADED MULTILEVEL INVERTER

As it can be seen, theExisting topology still uses a three-phase H-bridgeInverter supplied by a dc voltage and three single phaseH-bridge inverters. However, each arm of the three-phaseinverter has two outputs: one for the single-phase H-bridgeinverter and the other for the induction motorWinding.
In this way, it is possible to use a hybridmultilevel inverter applied to the induction motor withopen-end windings without using extra bridge inverters,power switches or power sources. This topology can alsowork as three single-phase multilevel inverters.

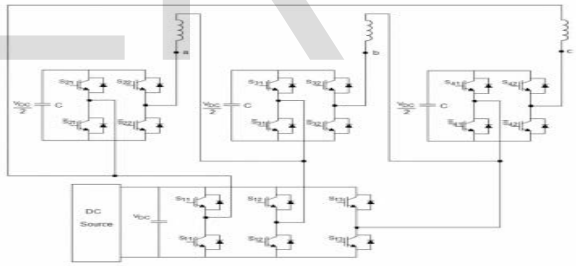

Fig 3.1 EXISTING H-BRIDGE MODEL

The existing system consists of a three phase inverter and three single phase inverters. Sliding mode control and sinusoidal pulse width modulation techniques are used. These techniques are complex and have several drawbacks. So we propose a 15 level inverter with H-bridge configuration alone. The proposed model uses Pulse Width Modulation (PWM) technique for controlling the gate pulses. In the proposed system DC supply for the inverters switches like MOSFET or IGBT is obtained from AC supply that is rectified. However renewable sources of energy can be used as a replacement for the AC supply used.

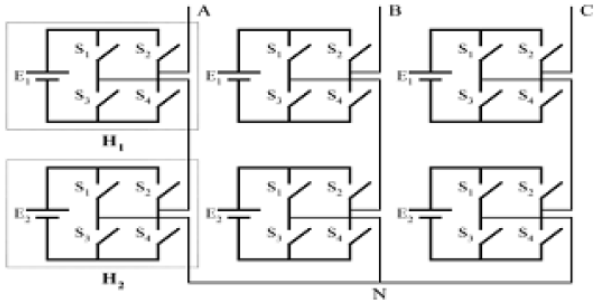

Fig 3.2 TOPOLOGY FOR A 5 LEVEL THREE PHASE INVERTER

The existing model shows the H-bridge configuration of a 5 level multilevel inverter. Based on the triggering gate pulses the switches conduct. Thus output is obtained in form of levels. [12]

In our paper we are presenting a H-bridge inverter model working on three phase AC supply. For real time implementation we are using MOSFET/IGBT as the switches. The control strategy is simple pulse width modulation technique (PWM) is used to control the gate pulses. Our model uses 7 H-Bridges of four power switches for synthesising a phase voltage.[12]

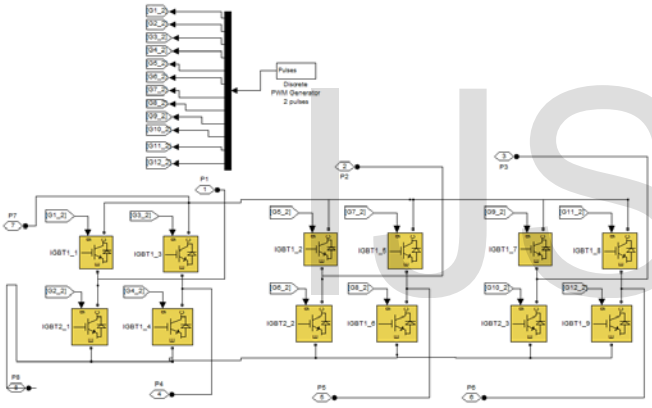

Fig 3.3 PROPOSED SUBSYSTEM FOR A SINGLE BLOCK

Each switch conducts for a particular time period based on the firing angle given to them. At any point of time only one switch is in conduction from one leg. No two switches from the same leg are in conduction at the same time. A pulse generator is implemented to provide width modulation and controlling the gate pulses.

The initial source for the inverter is existing AC supply. Using a three phase rectifier the AC voltage is converted to DC voltage. Suitable filters are used to get a undistorted waveform. This is fed to each inverter leg. Separate DC sources are added to each leg. The output voltage is the cumulative sum of phase voltage across each leg. In this way different legs are cascaded to synthesise the levels. Thus the H-bridge topology produces voltage levels obtained as a summation of individual voltages.

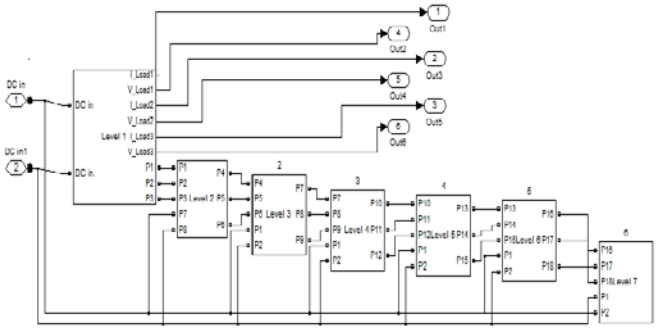

Fig 3.4 STRUCTURE OF OVERALL CASCADED H-BRIDGES

A capacitor may be added sometimes to split the DC source Voltage into two halves. The voltage across each capacitor is $V_{DC}/2$. In the proposed model 15 levels are synthesised using 7 sublevels of H-bridge with 28 switches for each phase of the three phase output. This comprises the circuit for DC to AC conversion using cascaded H-bridge inverter. Suitable filters are designed and added to the output so that a near sinusoidal three phase waveform is obtained.

4. CONTROL STRATEGY

The gate pulses are controlled using simple PWM technique. A pwm pulse generator is used to provide gate pulses for the gates of the switches. In this technique the width of the pulses are varied to vary firing angles of the thyristors. In pwm method the carrier wave and reference wave are superimposed on each other and compared. This logic serves as the difference in conduction of switches resulting in a pulsating AC output.

There are many forms of modulation used for communicating information. When a highfrequency signal has amplitude varied in response to a lower frequency signal we have AM(amplitude modulation). When the signal frequency is varied in response to the modulatingsignal we have FM (frequency modulation). These signals are used for radio modulation becausethe high frequency carrier signal is needs for efficient radiation of the signal. Whencommunication by pulses was introduced, the amplitude, frequency and pulse width becomepossible modulation options. In many power electronic converters where the output voltage canbe one

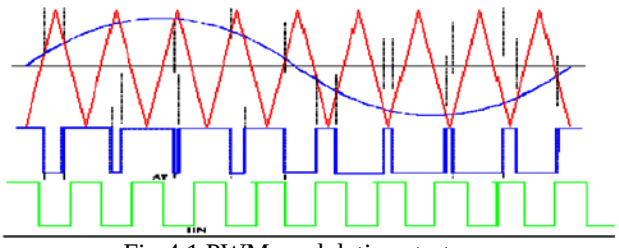

Fig 4.1 PWM modulation strategy

of two values the only option is modulation of average conduction time.[8]

The basic principle used for the pwm technique is:

PWM signal = sgn (r(t)-g(t))

Where r(t) – reference signal

g(t)-carrier signal

The simplest modulation to interpret is where the average ON time of the pulses varies proportionally with the modulating signal. The advantage of linear processing for this application lies in the ease of de-modulation. The modulating signal can be recovered from the PWM by low pass filtering. For a single low frequency sine wave as modulating signal modulating the width of a fixed frequency (fs) pulse train the spectra. In this manner all the switches are triggered based on the width of the pulses. However, PWM technique is the oldest technique. It is found that this technique has high THD value and result. Other techniques like POD technique can be used.

5. RESULTS:

To evaluate the dynamic performances of the proposedhybrid cascaded multilevel inverter and the control system, numerical simulations have been carried-out.The output voltage of the proposed multilevel inverter has fifteen levels. This is achieved due tothe relation between the amplitude of the DC voltagesource and the capacitors voltage. The DC voltage of thecapacitors is regulated to half the value of the DC source Voltage. The output waveforms are obtained by setting input voltage of 25KHZ AC that is converted to DC and inverted back to three phase AC. The output waveform has fifteen levels synthesised from the H-bridges. The peak value of voltages is clearly indicated. Harmonic analysis is also done to determine Total harmonic Distortion (THD).

From this result it is possible to verify that the Multilevel inverter provides near sinusoidal currents.

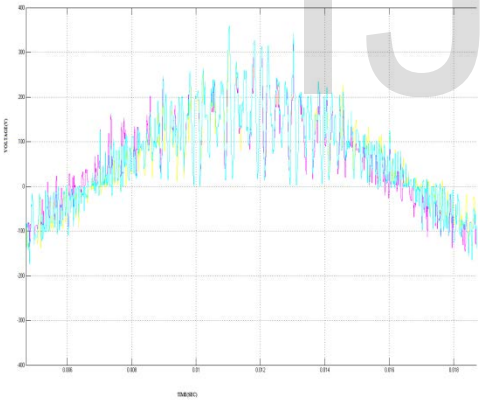

Fig 5.1 VOLTAGE WAVEFORM

The voltage waveform clearly shows the three phase output from the inverter model. The maximum amplitude of the voltage is 380V. The waveform is distorted as PWM technique is used. On close analysis the waveform for each phase is composed of levels or steps. Levels begin with + V_{DC} and -V_{DC} to required number of levels.. However a pure sinusoidal wave

is not obtained due to presence of harmonics. Filters may be used to reduce the distortion and get a near sinusoidal waveform. Some considerations to be noted are selection of snubber resistance and capacitance, magnetic inductance and reactance that are to be specified in transformer used for stepping down the input voltage.

FFT analysis is done to determine the THD value and waveform.

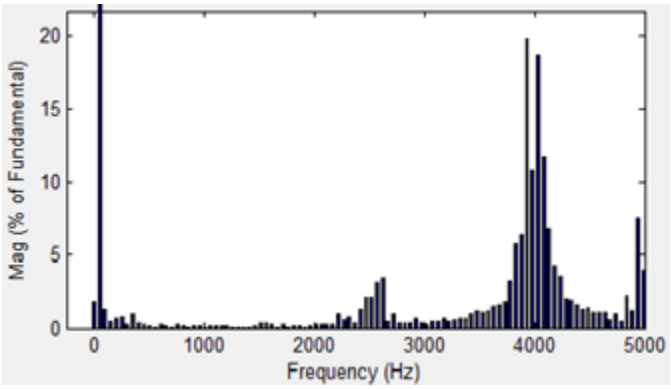

Fig 5.2 THD WAVEFORM

The harmonic analysis shows the presence of THD in fundamental components and other higher order components. The THD value at fundamental frequency is 22%.

In order to ensure the correctness of the simulation the output voltage is fed to a synchronous machine. The results obtained are shown.

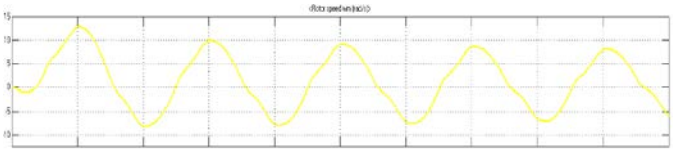

Fig 5.3 ROTOR SPEED

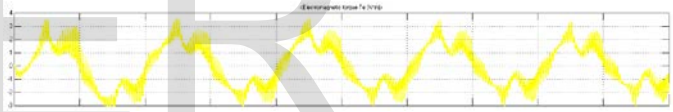

Fig 5.4 ELECTROMAGNETIC TORQUE

6.CONCLUSIONS:

In this paper fifteen level multilevel inveter is presented which uses PWM technique for controlling the gate pulses. In this design only cascaded H-bridge topology is used. This requires lower number of switches and components. Also THD can be reduced considerably in this method. DC source for switches are obtained from a AC source and given to each branch. However new control techniques like Phase Opposition Disposition, Space vector modulation can be also implemented. These methods provide a better THD value. Also as an innovation, an Hybrid H-bridge topology can be used for the h-bridges alone. The AC source may be replaced by a renewable energy input like a PV array, Hybrid power etc.

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